MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2016/2017

EEE4166 – DIGITAL INTEGRATED CIRCUIT

(All sections / Groups)

17 OCT 2016
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 6 pages with 4 questions only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\phi_T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\, R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) A simple diode circuit is shown in Figure Q1 (a).

(i) Assuming a silicon diode with $V_{D(on)} = 0.7$ V, determine current (I_1), voltage on R1 and R2 respectively.

(ii) If the voltage source V2 is removed and connected to ground, what are the new values for current (I_1) and voltage V_O?

[4+2 marks]

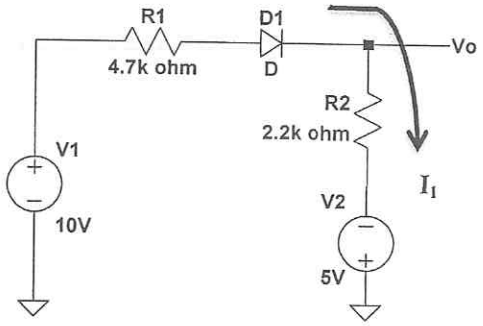

Figure Q1 (a)

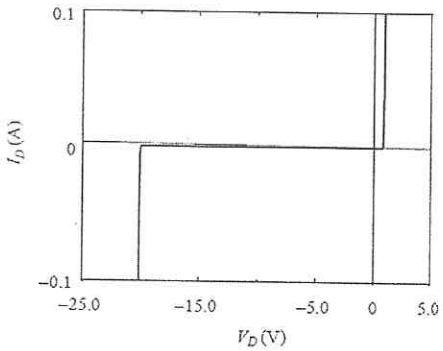

Figure Q1 (b)

(b) Referring to Figure Q1(b) above, describe the phenomena that happens when a bias voltage is applied across a diode.

[3 marks]

(c) In a generic 0.25 um CMOS process, the parameter values for a minimum sized NMOS transistor are given as threshold voltage, $V_{T0} = 0.43$ V, $-2\varphi_F = 0.8$ V, body effect coefficient, $\gamma = 0.4\ \sqrt{V}$ and $k_n' = 115\ \mu A/V^2$.

(i) An NMOS transistor with W/L = 4 is operating with $V_{SB} = 1.6$ V, $V_{GS} = 2$ V and $V_{DS} = 3$ V. Determine the operating region of this transistor and calculate its drain current, I_D.

(ii) From (i), calculate the drain current, I_D for a similar NMOS transistor which has the size of W/L = 40.

(iii)Based on (i) and (ii), comment on the relationship between these two transistors.

[8 marks]

(d) Understanding the second-order effects and their impact on an actual MOS transistor is essential in the design of digital circuits. Explain briefly FOUR second-order effects that can be found in a MOS transistor.

[8 marks]

Continued...

Question 2

(a) Referring to Figure Q2 (a) below, the inverter is truly the nucleus of all digital designs. Assume as output load of 5 pF, V_{T0} = 0.43 V, k_n' = 115 μA/V^2, V_{DD} = V_{OH} = 2.5 V, V_{OL} = 0.04 V and W/L for NMOS = 2/1.

(i) Describe TWO important properties of static CMOS inverter.

(ii) In Figure Q2 (a), replace the PMOS transistor with a 25 kΩ resistor to form a resistive load inverter. Calculate the propagation delays of t_{PLH}, t_{PHL} and t_P. During t_{PHL}, the average on resistance is 4 kΩ.

[4+5 marks]

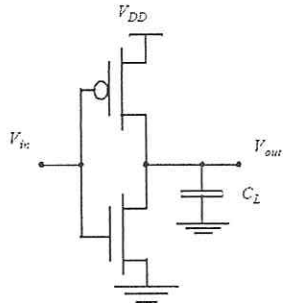

Figure Q2 (a)

(b) Given the function F below:

$$F = (A + B).\bar{C}$$

(i) Design a static CMOS gate realization of this function F with minimum transistor count. The input and inverted input ports are available for implementation.

(ii) From the design in Part (i), compute the W/L ratios of the transistors so that the output resistance is the same as that of an inverter with $(W/L)_{NMOS}$ = 1 and $(W/L)_{PMOS}$ = 4.

[6+4 marks]

(c) A monostable element is a circuit that generates a pulse of a predetermined width every time the quiescent circuit is triggered by a pulse or transition event. Sketch the circuit and describe the operation of the following monostable circuits.

(i) Transition-triggered circuit

(ii) RC-based triggered circuit

[6 marks]

Continued...

Question 3

(a) Design the Emitter-Coupled Logic (ECL) OR/NOR gate of the circuit in Figure Q3(a) below. The desired collector current is I_{C1} = 2 mA and V_{EE} = -5 V. At logic high, V_{OR} = -0.7 V, V_{NOR} = -1.6 V and VA = VB = -0.7 V. Assume V_{BE} = 0.7 V.

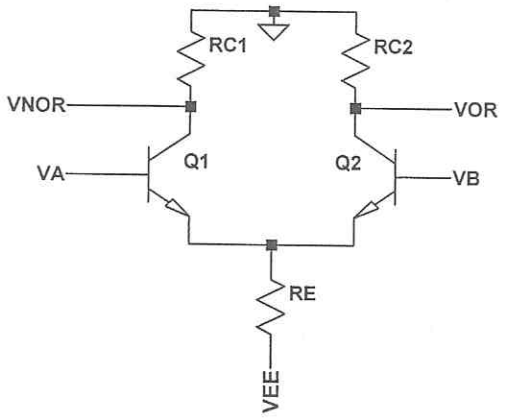

Figure Q3 (a) [11 marks]

(b) A BiCMOS inverter circuit is shown in Figure Q3(b) below. It has V_{DD} = 3 V, V_{BE} = 0.7 V, R_1 = 2 kΩ, R_2 = 5 kΩ, C_L = 1 pF and β =100. As for CMOS, the threshold voltages V_{tp} = -0.5 V, V_{tn} = 0.5 V and K_p = 20 μA/V^2. Assume V_{OL} = 0 V and V_{OH} = 3 V.

(i) Calculate t_{pLH}, t_{pHL} and t_{pd}.

(ii) Describe the operation of the BiCMOS inverter circuit when input voltage v_I applied is LOW (at V_{OL}).

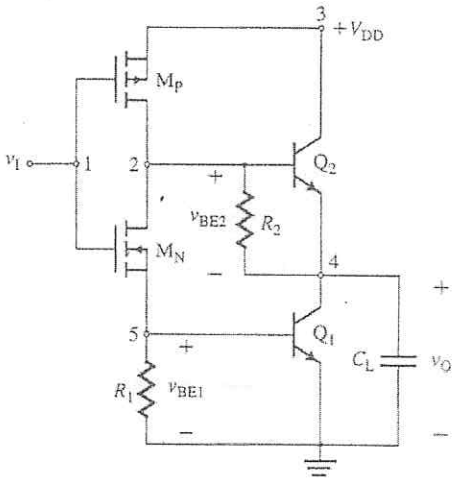

Figure Q3(b) [8+6 marks]

Continued...

Question 4

(a) For the following function:

$$F = A + (\overline{B.C})$$

(i) Implement the F function with static CMOS gates.

(ii) Based on circuit drawn in part (i), determine the dynamic power consumption, P_{dyn} of the circuit. Given the load capacitance, C_L = 100 fF, voltage supply, V_{DD} = 5 V and clock frequency, f_{clk} = 100 MHz. Assume that the input signals are random.

Hint: Use a truth table

[14 marks]

(b) Ideally, the static power consumption of the CMOS inverter is equal to zero. However in reality, there is always a leakage current present. Describe the phenomena which cause such current to exist and how it contributes to the power consumption.

[3 marks]

(c) Power dissipation consists of a static component and a dynamic component. By far, dynamic power is the dominant component in CMOS circuits.
Propose TWO methods to reduce dynamic power dissipation in a circuit.

[4 marks]

(d) Figure Q4 below shows a Table of the technology roadmap for semiconductors. Based on this Table, critic and predict the future of semiconductor for next year, 2017.

year	2001	2004	2007	2010	2013	2016
size [nm]	130	90	65	45	32	22
V_{DD}[V]	1.1–1.2	1–1.2	0.7–1.1	0.6–1.0	0.5–0.9	0.4–0.9
MT/die	193	385	773	1564	3092	6184
Wire levels	8–10	9–13	10–14	10–14	11–15	11–15
I/O signals	1024	1024	1024	1280	1408	1472
Frequency [MHz]	1684	3990	6739	11511	19348	28751
FO4 delays/cycle	13.7	8.4	6.8	5.8	4.8	4.7
Max. power [W]	130	160	190	218	251	288
DRAM size [Gb]	0.5	1	4	8	32	64

Figure Q4

[4 marks]

End of Paper